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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,596	07/23/2004	Mou-Shiung Lin	085027-0101	4595

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McDermott Will & Emery LLP  
11682 El Camino Real  
Suite 400  
San Diego, CA 92130

EXAMINER
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MATTHEWS, COLLEEN ANN

ART UNIT	PAPER NUMBER
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2811

NOTIFICATION DATE	DELIVERY MODE
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08/05/2010

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

SIP\_Docket@mwe.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/710,596	<b>Applicant(s)</b> LIN, MOU-SHIUNG	
	<b>Examiner</b> Colleen A. Matthews	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 43-74, 83, 84 and 89-102 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 43-74, 83-84 and 89-102 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 43 and 89 are rejected under 35 U.S.C. 102(b)** as being anticipated by U.S. Pat. No. 5,328,553 to Poon.

**Re claim 43:** Poon discloses a chip structure (Fig 5) comprising:

a silicon substrate (50);

a resistor (51, 52 or 53; col 5 lines 33-37, considered as 51 for example) in said silicon substrate, wherein said resistor comprises silicon with a dopant (col 5 lines 33-37),

a MOS device (51, 52 or 53; col 5 lines 33-37) comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer (26) and a second metal layer (30) over said first metal layer;

a first dielectric (36) layer between said first and second metal layers;

a passivation layer (38) over the metallization structure and over said dielectric layer, wherein a first opening (40) in said passivation layer is over a first contact point (corresponding to doped region 51) of a first metal interconnect of said metallization

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structure and said first contact point is at a bottom of said first opening, and a second opening (40) in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure and said second contact point is at a bottom of said second opening, wherein a gap (created by passivation layers 34, 36, 38) is between said first and second metal interconnects, wherein said first contact point is connected to said resistor (51), wherein said passivation layer comprises an insulating nitride layer (col 5 lines 62-68); and

a circuit trace (42) over the passivation layer and on said first and second contact points (40), wherein said first contact point is connected to said second contact point through said circuit trace (42).

**Re claim 89:** Poon discloses a chip structure (Fig 5) comprising:

a silicon substrate (50);

a resistor (51, 52 or 53; col 5 lines 33-37, considered as 51 for example) in said silicon substrate, wherein said resistor comprises silicon with a dopant (col 5 lines 33-37),

a MOS device (51, 52 or 53; col 5 lines 33-37) comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer (26) and a second metal layer (30) over said first metal layer;

a dielectric (36) layer between said first and second metal layers;

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a passivation layer (38) over the metallization structure and over said dielectric layer, wherein a first opening (40) in said passivation layer is over a first contact point (corresponding to doped region 51) of a first metal interconnect of said metallization structure and said first contact point is at a bottom of said first opening, and a second opening (40) in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure and said second contact point is at a bottom of said second opening, wherein a gap (created by passivation layers 34, 36, 38) is between said first and second metal interconnects, wherein said first contact point is connected to said resistor (51), wherein said passivation layer comprises an insulating nitride layer (col 5 lines 62-68); and

a circuit trace (42) over the passivation layer and on said first and second contact points (40), wherein said first contact point is connected to said second contact point through said circuit trace (42), wherein said circuit trace comprises a copper layer (copper, col 6 lines 12-13).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 54-59 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 5,328,553 to Poon in view of U.S. Pat. No. 6,235,101 to Erdejac et al. (Erdejac).

**Re claims 54-58:** Poon discloses the circuit structure as claimed in 43. Poon fails to explicitly disclose the structure comprising an inductor over said passivation layer where said inductor comprises a copper layer.

Erdejac teaches an inductor (top metal inductor Fig 20c) over said passivation layer where said inductor comprises: a copper layer (col 6 lines 65-68); a gold layer (col 7 line 25-26); or a titanium-tungsten alloy layer and a copper layer over said titanium-tungsten alloy layer (col 6 lines 57-60).

Poon and Erdejac are analogous art because both are directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to have the inductor as in Erdejac in order to create a circuit structure for specific applications such as RF.

**Re claim 59:** Poon discloses the circuit structure as claimed in 43. Poon fails to explicitly disclose the structure comprising a capacitor over said silicon substrate.

Erdejac teaches a capacitor (Fig 20b, poly poly capacitor) over said silicon substrate, a second dielectric layer (between poly 0 and poly 1) on said first electrode (poly 0) and in the third opening, a second electrode (poly 1) on said second dielectric layer and over said first electrode.

Poon and Erdejac are analogous art because both are directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to include the capacitor as in Erdejac in order to create a circuit structure for specific applications such as RF.

**Claims 64, 60-63, 69-74, 83-84 and 100-102 are rejected under 35 U.S.C.**

**103(a)** as being unpatentable over U.S. Pat. No. 5,328,553 to Poon in view of U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) or U.S. Pat. No. 5,328,553 to Poon in view of U.S. Pat. No. 6,235,101 to Erdejac et al. (Erdejac) and U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa).

**Re claim 64:** Poon discloses a chip structure (Fig 5) comprising:

a silicon substrate (50);

a resistor (51, 52 or 53; col 5 lines 33-37, considered as 51 for example) in said silicon substrate, wherein said resistor comprises silicon with a dopant (col 5 lines 33-37),

a MOS device (51, 52 or 53; col 5 lines 33-37) comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer (26) and a second metal layer (30) over said first metal layer;

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a dielectric (36) layer between said first and second metal layers;

a passivation layer (38) over the metallization structure and over said dielectric layer, wherein a first opening (40) in said passivation layer is over a first contact point (corresponding to doped region 51) of a first metal interconnect of said metallization structure and said first contact point is at a bottom of said first opening, and a second opening (40) in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure and said second contact point is at a bottom of said second opening, wherein a gap (created by passivation layers 34, 36, 38) is between said first and second metal interconnects, wherein said first contact point is connected to said resistor (51), wherein said passivation layer comprises an insulating nitride layer (col 5 lines 62-68); and

a circuit trace (42) over the passivation layer and on said first and second contact points (40), wherein said first contact point is connected to said second contact point through said circuit trace (42).

Poon fails to disclose where said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

Sasagawa teaches a circuit trace (109-111) comprises a titanium-containing layer (109, col 4 line 14 ) and a gold layer (111, col 4 line 21) over said titanium-containing layer.

Poon and Sasagawa re analogous art because both a directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.



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It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to include the different circuit trace and metallization layers of Sasagawa in order to optimize the device performance under thermal stress.

**Re claims 60-63, 83-84 and 100-102:** Poon as modified discloses the device of 43, 65 and 89 as above. Poon fails to disclose the circuit trace/second electrode comprising, aluminum or a gold layer over the copper layer, a titanium layer under the copper layer, a titanium-containing layer comprising tungsten, a chromium layer under the copper layer, a gold layer, a titanium-containing layer under gold layer and a titanium-containing layer comprising tungsten.

Sasagawa teaches a circuit trace/capacitor second electrode (109-111) comprises aluminum, or nickel layer over a copper layer and the circuit trace comprising a gold layer over the copper layer, a titanium layer under the copper layer, a chromium layer under the copper layer, a gold layer, a titanium-containing layer under gold layer and a titanium-containing layer (col 4 lines 13-22). Erdejac teaches a titanium-containing layer comprising a titanium-tungsten alloy (col 6 lines 57-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to include the different circuit trace and metallization layers of Sasagawa and Erdejac in order to optimize the device performance under thermal stress.

**Claims 48-53, 69-74, and 94-99 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 5,328,553 to Poon as applied to claims 44 and 89

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above and U.S. Pat. No. 5,328,553 to Poon in view of U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) as applied to claim 64 above and in view of U.S. Pat. No. 6,495,442 to Lin et al (Lin).

**Re claims 48-53 and 94-99:** Poon discloses the device as above. Poon fails to disclose a polymer layer on the passivation. Lin teaches a polymer layer (20) on the passivation layer (18) and the circuit trace (26/22/21/36/28) and wherein said circuit trace is further on the polymer layer and the polymer layer comprises polyimide (PI) or benzocyclobutene (BCB), (col 5, lines 19 and 23-27).

Poon and Lin are analogous art because both are directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to include the polymer layer and materials taught by Lin in order to protect the chip structure from contamination.

**Re claims 69-74:** Poon discloses the device as above. Poon fails to disclose a polymer layer on the passivation. Lin teaches a polymer layer (20) on the passivation layer (18) and the circuit trace (26/22/21/36/28) and wherein said circuit trace is further on the polymer layer and the polymer layer comprises polyimide (PI) or benzocyclobutene (BCB), (col 5, lines 19 and 23-27).

Poon and Lin are analogous art because both are directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to include the polymer layer and materials taught by Lin in order to protect the chip structure from contamination.

**Claims 44-46, 65-67, 90-92 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 5,328,553 to Poon as applied to claims 44 and 89 above and U.S. Pat. No. 5,328,553 to Poon in view of U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) as applied to claim 64 above and in further view of U.S. Pub. No. 2003/0155570 to Leidy.

**Re claims 44-46, 65-67, 90-92**, Poon discloses the device of 43, 65, and 89 as above including the resistor comprising silicon with a dopant (col 5 lines 33-37). Poon fails to disclose the resistor comprising a dopant of boron or phosphorous.

Leidy teaches a resistor comprising silicon and a dopant of boron, phosphorous, or arsenic (page 5, claim 26).

Poon and Leidy are analogous art because both are directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to have the resistor made of silicon and a dopant of boron, phosphorous, or arsenic as in Leidy in order to be able to predetermine the device resistivity (Leidy, page 3, paragraph 37).

**Claims 45, 47, 66, 68, 91 and 93 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 5,328,553 to Poon as applied to claims 44 and 89 above and U.S. Pat. No. 5,328,553 to Poon in view of U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) as applied to claim 64 above and in further view of U.S. Pub. No. 2003/0183332 to Simila.

**Re claims 45, 47, 66, 68, 91 and 93:** Poon discloses the device of 43, 65 and 89 as above including the resistor comprising silicon with a dopant (col 5 lines 33-37). Poon fails to disclose the resistor comprising a dopant of phosphorous or gallium.

Simila a resistor comprising silicon and a dopant of phosphorous or gallium (paragraph 70).

Poon and Simila are analogous art because both are directed to chip structures with metallization and one of skill in the art would have had a reasonable expectation of success to combine references because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Poon to have the resistor made of silicon and a dopant of phosphorous or gallium as in Simila in order to be able to predetermine the device resistivity.

### ***Response to Arguments***

Applicant's arguments with respect to claims 43-74, 83-84 and 89-102 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is (571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Colleen A Matthews/  
Examiner, Art Unit 2811

/Lynne A. Gurley/  
Supervisory Patent Examiner, Art  
Unit 2811